Amendments to the Specification:

Amendments to the Specification are shown below.

Please replace the paragraph bridging pages 3 and 4 of the Specification, with the following amended paragraph:

In accordance with the present invention a method of defining a contact or via opening in a stack of insulator layers featuring an underlying tri-layer insulator composite, used as a stop layer during the dry etch contact opening definition procedure, is described. A tri-layer insulator composite comprised of an underlying silicon rich oxide layer, a hydro-silicon oxynitride ~~(HOxSN)~~ (SiOxNH) layer, and an overlying silicon nitride layer, is formed on the surface of a conductive or insulator region of an underlying semiconductor device. A boro-phosphosilicate glass (BPSG) layer and an overlying silicon oxide layer are next deposited on the tri-layer composite. After application of a bottom anti-reflective coating (BARC) layer, a photoresist shape is defined, and used as an etch mask to allow an anisotropic reactive ion etch (RIE) procedure to define the desired contact or via opening in the silicon oxide and BPSG layers, with the dry etch procedure terminating in the silicon nitride component of the tri-layer composite. A critical over etch cycle is then employed to insure a complete removal of insulator (BPSG and silicon oxide), accomplished a result of the high etch rate selectivity of silicon oxide to silicon nitride. Selective removal of silicon nitride via an anisotropic RIE procedure is followed by selective removal of the ~~HOxSN~~ SiOxNH component, with the dry etch procedure slowing at the appearance of the silicon rich oxide component of the tri-layer composite. Removal of the silicon rich oxide layer via a continuation of the anisotropic RIE procedure is selectively accomplished exposing a

portion of the top surface of an conductive or insulator region of a semiconductor device.

Please replace the paragraph beginning on line 2 of page 5 with the following amended paragraph:

The method of defining a contact or via opening in a stack of insulator layers featuring an underlying tri-layer insulator composite used as an etch stop layer, will now be described in detail. For description purposes Figs. 1 - 6, will show key stages used to define of an opening in a stack of insulator layers employing the novel underlying tri-layer etch stop component wherein the opening is shown exposing a top portion of a isolation region. However the same openings, contact or via openings, are shown in Fig. 7 - 8, exposing conductive regions of a semiconductor device. Semiconductor 1, comprised of single crystalline silicon, featuring a <100> crystallographic orientation, is used and schematically shown in Fig. 1. Isolation region 2, an element such as an insulator filled, shallow trench isolation (STI) region is formed in a top portion of semiconductor substrate 1. The STI region can be comprised of silicon oxide. If desired isolation region 2, can be a thermally grown, silicon dioxide field oxide (FOX) region. Formation of the tri-layer insulator composite, to be used as an etch stop during definition of a subsequent contact or via opening, is addressed. First silicon rich[[,]]-silicon oxide layer 3, is formed to a thickness between about 100 to 200 Angstroms via plasma enhanced chemical vapor deposition (PECVD), via low pressure chemical vapor deposition (LPCVD), or via high density plasma chemical vapor deposition (HDPCVD) procedures. The deposition is performed using a ratio of silane or disilane, to oxygen or nitrous oxide, that results in a refractive index for silicon rich[[,]]-silicon oxide layer 3,

between about 1.485 to 1.55. The silicon rich feature of silicon oxide layer 3, will allow a desired etch rate selectivity to be realized during the definition of the contact or via opening. A liner layer comprised of ~~(HOxSN)~~ (SiOxNH) layer 4, is next formed via PECVD, LPCVD, or HDPCVD procedures, at a thickness between about 200 to 500 Angstroms. Finally silicon nitride layer 5, to be used as the etch stop component of the tri-layer insulator composite during the definition and over etch cycles of overlying insulator layers, is deposited to a thickness between about 100 to 200 Angstroms via PECVD, LPCVD, or HDPCVD procedures. The result of formation of the tri-layer insulator composite, comprised of overlying silicon nitride layer 5, ~~(HOxSN)~~ (SiOxNH) layer 4, and underlying silicon rich, silicon oxide layer 3, are shown schematically in Fig. 1. The thicker overlying dielectric layers used for the bulk of insulation between conductive interconnect levels or between a conductive level and a conductive region in the semiconductor substrate, are next formed. Boro-phosphosilicate glass (BPSG) layer 6, is obtained at a thickness between about 1500 to 2500 Angstroms, via PECVD or LPCVD procedures. This is followed by formation of overlying silicon oxide layer 7, obtained at a thickness between about 5000 to 6000 Angstroms, again via PECVD or LPCVD procedures, using tetraethylorthsilicate (TEOS) as a source. This is also schematically shown in Fig. 1.

Please replace the paragraph bridging pages 7-8 of the Specification with the following amended paragraph:

Selective removal of the tri-layer insulator composite is next addressed and schematically described using Figs 5 - 6. The anisotropic RIE procedure used to define

the desired opening in silicon oxide layer 7, and in BPSG layer 6, and used to supply the desired over etch cycle, is now continued using CF_4 or Cl_2, as a selective etchant for silicon nitride layer 5, and for ~~HOxSN~~ (SiOxNH) layer 4, resulting in opening 10d, schematically shown in Fig. 5. The higher etch rate of silicon nitride and ~~HOxSN~~ SiOxNH layer 4, in CF_4, when compared to silicon rich, silicon oxide layer 3, allows this cycle to terminate in silicon rich[[,]]-silicon oxide layer 3. The anisotropic RIE procedure is now continued, again using CHF_3 as an enchant, allowing exposed portions of silicon rich[[,]] - silicon oxide layer 3, to be removed resulting in opening 10e, exposing a portion of the top surface of STI region 2. The use of the tri-layer insulator composite, featuring stop layer properties, allowed the needed over etch cycle to be employed without risk of etching or penetrating into the underlying material, STI region 2, in this case. Photoresist shape 9, as well as BARC layer 8, are now removed via plasma oxygen ashing procedures. This is schematically shown in Fig. 6.

Please replace the paragraph bridging pages 8-9 of the Specification with the following amended paragraph:

The process illustrated in Figs. 1 - 6, featured a generic description of a procedure used to define a contact or via opening in a stack of insulator layers comprised with an underlying tri-layer insulator composite used as a stop layer for the dry etch definition procedure. Fig. 7, schematically shows an example of this invention in which borderless contact opening 10f, is formed with the above dry etch definition procedure. The stop layer properties of the tri-layer insulator composite allowed the selective anisotropic RIE procedure to expose a portion of a top surface of conductive region 11, without gouging or penetration at the surface of the conductive region.

Conductive region 11, can be a source/drain region, or a metal silicide layer formed on an underlying area such as a source/drain region. Another example of the use of the tri-layer insulator composite as a component of an insulator stack is shown schematically in Fig, 8, wherein via opening 10g, is defined using an anisotropic RIE procedure. The presence of the tri-layer insulator composite, comprised of silicon nitride layer 5, ~~(HOxSN)~~ (SiOxNH) layer 4, and silicon rich[[,]]-silicon oxide layer 3, allowed the dry etch procedure to successfully define via opening 10g, while terminating at the appearance of a portion of a top surface of conductive region 12, wherein conductive region 12, can be a metal interconnect structure.